REMARKS

This is a full and timely response to the outstanding final Office Action mailed August 22, 2006. Upon entry of the amendments in this response, claims 1, 3 – 12, 14 – 19, 22, 25 and 26 are pending. In particular, Applicants have amended claims 1 and 10. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

Rejections Under 35 U.S.C. §112, Second Paragraph

The Office Action rejects claims 1 – 8, 10, 19 and 22 under 35 U.S.C. 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. In this regard, Applicants have amended claims 1 and 10 and respectfully assert that the rejections have been rendered moot. With respect to the rejections of claims 19 and 22, Applicants respectfully assert that it appears as though the Office Action has considered the language of claims 19 and 22 prior to the entry of Applicant's last amendments. Specifically, the Office Action appears to be rejecting these claims based on language that is not recited in the pending claims. Further clarification is requested.

Rejection Under 35 U.S.C. §112, First Paragraph

The Office Action rejects claims 1 - 8 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. In this regard, the Office Action indicates that "transferring at least some of the data into the buffer. . ." is not supported by the specification. Notably, the transfer of data is clearly described as a potentially iterative process involving transfer of some of the data that is to be transfer during each iteration. Such teachings support the recitation of transferring at least some of the data. Regardless,

Applicants have amended claim 1 and respectfully assert that the rejection has been rendered moot.

Rejections Under 35 U.S.C. §101

The Office Action indicates that claims 1, 3 – 12, 14 – 19, 22 and 25 - 26 stand rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. In particular, the Office Action alleges that claims 1, 3 – 12, 14 – 19, 22 and 25 – 26 do not support the preamble and that they appear to define non-statutory processes. Applicants respectfully traverse.

With respect to claims 10 – 12, and 14 – 18, these claims are directed to a data transfer system comprising, among other, various registers, a buffer and a host interface. Clearly, these claims do not recite a process, much less a non-statutory process. Additionally, the recited elements are coordinated with the environmental features recited in the preamble, i.e., the host device and the storage medium. Therefore, the rejection appears to be misplaced and removal is respectfully requested.

With respect to claim 22, that claim is directed to an application specific integrated circuit (ASIC), i.e., an apparatus and/or an article of manufacture. Clearly, these claims do not recite a process, much less a non-statutory process. Additionally, the recited elements are coordinated with the environmental features recited in the preamble, i.e., the host device and the storage medium. The Office Action appears to indicate that an ASIC is software, apparently disregarding the fact that Applicant has claimed the component, which comprises a buffer and first and second registers (also structural features), not merely the functionality involved. Therefore, the rejection appears to be misplaced and removal is respectfully requested.

With respect to claims 1, 3 – 9, 25 and 26, these claims are directed to a method for transferring data between a host device and a storage medium via a buffer. Clearly, these claims recite a statutory process that involves the transfer of data between physical components, thereby manifesting a tangible result. Additionally, the recited elements are coordinated with the environmental features recited in the preamble, i.e., the host device and the storage medium. Therefore, the rejection appears to be misplaced and removal is respectfully requested.

Rejections Under 35 U.S.C. §102

The Office Action indicates that claims 1 and 7 - 9 stand rejected under 35 U.S.C. 102(b) as being anticipated by *Siegel*. Applicants respectfully traverse the rejections.

With respect to *Siegel*, *Siegel* teaches the use of a base count register that keeps track of the number of bytes that are left to be transferred. However, in order to determine whether transferred data is present in a buffer during a transfer, a decision is made whether the cache RAM buffer address corresponding to the address of the DMA controller 36 currently contains transferred data. Thus, *Siegel* analyzes address usage to monitor data transfer to the buffer. This is in direct contrast to the limitations recited in Applicants' claims that generally involve the use of registers to track such transfers. Moreover, Applicants respectfully assert that it is improper to attribute any teaching of a buffer to Applicants' claimed register, as Applicants have clearly and distinctly recited a buffer in addition to a register.

In this regard, Applicants have amended claim 1 to recite:

> 1. A method for transferring data between a host device and a storage medium via a buffer, comprising:
> receiving from the host device a command to transfer data between the host device and the storage medium;
> ***storing in a first register a value for tracking a number of sectors in the buffer available for storing data units***;

> ***storing in a second register a value corresponding to a number of data units to be transferred during an iteration of the transfer of the data between the host device and the storage medium***;
>
> transferring the number of the data units into the buffer from one of the host device and the storage medium responsive to the command;
>
> ***modifying the value contained in the first register with the value stored in the second register in response to a completed iteration of the transfer of the data into the buffer***;
>
> transferring the number of the data units out of the buffer and to another of the host device and the storage medium; and
>
> ***modifying the value contained in the first register in response to a transfer of the data units out of the buffer***;
>
> ***wherein, during the transfer of the data between the host device and the storage medium, the value contained in the first register corresponds to a number of data units currently stored in the buffer.***

(Emphasis Added).

Applicants respectfully assert that *Siegel* is legally deficient for the purpose of anticipating claim 1. Specifically, Applicants respectfully assert that *Siegel* does not teach or otherwise disclose at least the features/limitation emphasized above in claim 1. In this regard, *Siegel* analyzes address usage to monitor data transfer to the buffer and is not involved with "modifying the value contained in the first register with the value stored in the second register in response to a completed iteration of the transfer of the data into the buffer," as recited in claim 1. Therefore, Applicants respectfully assert that the rejection is improper and requests that the claim 1 be placed in condition for allowance.

Since claims 7 - 9 are dependent claims that incorporate the limitations of claim 1, Applicants respectfully request that the rejection of the claims under 35 U.S.C. 102(b) also be removed.

Rejections Under 35 U.S.C. §103

The Office Action indicates that claims 3 – 6, 10 – 12, 14 – 19, 22 and 25 – 26 stand rejected under 35 U.S.C. 103(a) as being unpatentable over *Siegel* and *Sefidvash*. Applicants respectfully traverse.

With respect to claims 3 – 6 , 25 and 26, *Sefidvash* does not remedy the aforementioned deficiencies of *Siegel*. Since these claims incorporate the limitations recited in claim 1, Applicants respectfully assert that these claims also are in condition for allowance for at least this reason.

With respect to claim 10, Applicants have amended claim 10 to recite:

> 10. A data transfer system for transferring data between a host device and a storage medium, comprising:
>
> a host interface operative to receive from the host device a command to transfer data between the host device and the storage medium;
>
> a buffer operative to temporarily store data that is transferred between the host device and the storage medium;
>
> ***a first register operative to store a value for tracking a number of sectors in the buffer available for storing data units***; and
>
> ***a second register operative to store a value for modifying the value contained in the first register, the value stored in the second register corresponding to a number of data units to be transferred during an iteration of the transfer of the data between the host device and the storage medium***;
>
> ***wherein, in transferring the data between the host device and the storage medium, the value contained in the first register corresponds to a number of data units currently stored in the buffer.***

(Emphasis Added).

Applicants respectfully assert that *Siegel* and *Sefidvash*, either individually or in combination, are legally deficient for the purpose of rendering claim 10 unpatentable. Specifically, Applicants respectfully assert that the combination does not teach or reasonably suggest at least the features/limitation emphasized above in claim 10. Therefore, Applicants respectfully assert that the rejection is improper and requests that the claim 10 be placed in condition for allowance.

Since claims 11, 12 and 14 - 18 are dependent claims that incorporate the limitations of claim 10, Applicants respectfully request that the rejection of these also be removed.

In this regard, claim 19 recites:

> 19. A method for transferring data between a host device and a storage medium via a buffer, comprising:
> receiving from the host device a command to transfer data between the host
> device and the storage medium;
> ***storing in a first register a value indicative of an amount of data that can be currently stored in the buffer;***
> ***incrementing the value contained in the first register by a value contained in a second register in response to an iteration of a data transfer into the buffer, the value in the second register corresponding to a number of data units to be transferred during the iteration of the transfer of the data between the host device and the storage medium; and***
> ***decrementing the value contained in the first register in response to a data transfer out of the buffer.***

(Emphasis Added).

As an initial matter, it appears that the Office Action has re-examined the claim language previously recited in claim 19. That is, the Office Action refers to "a buffer's fullness" as being recited in claim 19; however, that language was amended in Applicants' previous response. Further clarification is respectfully requested.

As the pending rejection is best understood by Applicants, Applicants respectfully assert that *Siegel* and *Sefidvash*, either individually or in combination, are legally deficient for the purpose of rendering claim 19 unpatentable. Specifically, Applicants respectfully assert that the combination does not teach or reasonably suggest at least the features/limitation emphasized above in claim 19. That is, neither reference appears to teach at least "incrementing the value contained in the first register by a value contained in a second register in response to an iteration of a data transfer into the buffer." Therefore, Applicants respectfully assert that the rejection is improper and requests that the claim 19 be placed in condition for allowance.

In this regard, claim 22 recites:

> 22. An application specific integrated circuit (ASIC) for transferring data between a host device and a storage medium, comprising:
>
> a buffer that temporarily stores data that is transferred between the host device and the storage medium;
>
> ***a first register that stores a value corresponding to an amount of data that can be currently stored in the buffer; and***
>
> ***a second register that stores a value corresponding to a number of data units to be transferred to the buffer such that, responsive to the number of data units being transferred into the buffer, the value stored in the first register is incremented with the value contained in the second register;***
>
> ***wherein, in response to a data transfer out of the buffer, the value contained in the first register is decremented by a value corresponding to a number of data units transferred out of the buffer.***

(Emphasis Added).

As an initial matter, it appears that the Office Action has re-examined the claim language previously recited in claim 22. That is, the Office Action refers to "a buffer's fullness" as being recited in claim 22; however, that language was amended in Applicants' previous response. Further clarification is respectfully requested.

As the pending rejection is best understood by Applicants, Applicants respectfully assert that *Siegel* and *Sefidvash*, either individually or in combination, are legally deficient for the purpose of rendering claim 22 unpatentable. Specifically, Applicants respectfully assert that the combination does not teach or reasonably suggest at least the features/limitation emphasized above in claim 22. That is, neither reference appears to teach at least "responsive to the number of data units being transferred into the buffer, the value stored in the first register is incremented with the value contained in the second register." Therefore, Applicants respectfully assert that the rejection is improper and requests that the claim 22 be placed in condition for allowance.

Cited Art Made of Record

The cited art made of record has been considered, but is not believed to affect the patentability of the presently pending claims.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicants respectfully submit that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,

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on 10/23/06.

Stephanie Riley
Signature